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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/576,348

04/18/2006

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EXAMINER

STEVENS, GERALD D

ART UNIT

PAPER NUMBER

2817

NOTIFICATION DATE

DELIVERY MODE

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ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

<b>Office Action Summary</b>	<b>Application No.</b> 10/576,348	<b>Applicant(s)</b> KAWAKAMI ET AL.	
	<b>Examiner</b> GERALD STEVENS	<b>Art Unit</b> 2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 12 February 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1,3,5,7,8,10,12 and 14-28 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,3,5,8,10,12 and 15-28 is/are rejected.
- 7) ☒ Claim(s) 7 and 14 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 April 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)            | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | Paper No(s)/Mail Date. _____                                      |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>04/18/2006</u>  | 6) <input type="checkbox"/> Other: _____                          |

### **DETAILED ACTION**

1. This action is in response to the communications filed on 12 February 2008.
2. Claims 1, 3,5,7,8,10,12,14, & 15-28 are pending. Claims 1,3,5,7,8,10,12, & 14 are amended, claims 14-28 being new, & claims 2,4,6,9,11, & 13 are cancelled.

### ***Response to Arguments***

1. Applicant's arguments with respect to claims 1 & 8 have been considered and are addressed in the new statement of rejection below.

### ***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1, 3, 5, 8, 10, 12, 15, 16, 19, 20, 25, & 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Belfatto (US 4266201) in view of Connerney et al (US 4955079).

Regarding claims 1 & 8, Belfatto teaches branching means (sole fig. resistor 38, wherein the connection points between pulse source 34 and mixer 12 is the branching means) for receiving a pulsed signal from a pulse applying terminal (sole fig. source 34) and

also a branching means (sole fig. splitter 16, inverter 26, and delay 42, wherein the connection points between carrier source 10 and mixers 48 & 12 are branching means) for receiving a local oscillation signal from a local oscillation wave input terminal (sole fig. source 10, wherein the carrier frequency is the local oscillation source), and

branching means (sole fig. combiner 66, attenuators 54, 56, wherein the connection points between mixers 28, 48 and the output terminal are branching means) for outputting a pulsed signal;

a mixing means (sole fig. mixer 28) for mixing the pulsed signal (sole fig. output of pulse source 34) delivered thereto by said branching means (sole fig. connection points between mixer 12 and pulse source 34) and the local oscillation signal (sole fig. output of source 10); and

a voltage dividing means (sole fig. resistor 38) for dividing a voltage applied to said mixing means (col. 2 lines 40-42, wherein setting the proper voltage level is dividing the applied voltage),

but fails to teach furnishing a pulsed signal having a frequency even times the frequency of the local oscillation signal to said branching means and the output pulsed signal having a frequency even times a frequency of the local oscillation signal.

Connerney teaches furnishing an rf signal (fig. 1 signal "RADIO FREQUENCY SIGNAL") having a frequency even times (col. 2 lines 39-45) the frequency of the local oscillation signal (fig. 1 oscillator signal "LOCAL OSCILLATOR SIGNAL") to said branching means (fig. 1 branches 14, 16) and

the output signal (fig. 1 signal "IF SIGNAL") having a frequency even times a frequency of the local oscillation signal (fig. 1 signal "LOCAL OSCILLATOR SIGNAL", col. 2 lines 45-47).

It would have been obvious to one having ordinary skill in the art at the time of the invention to have substituted the modulation input pulse source as taught by Belfatto with the rf signal source as taught by Connerney because it is obvious to substitute an art equivalent signal source such as taught in Connerney in the place of a generic signal source as shown in Belfatto.

Regarding claims 3 & 10, Belfatto further teaches said resistor (sole fig. resistor 38) comprising said voltage dividing means (sole fig. resistors 36,38,40, col. 2 lines 40-42) being a variable resistor (sole. fig. resistor 52).

Wherein it would have been obvious to one having ordinary skill in the art at the time of the invention to have modified the biasing resistor as taught in the sole figure with the equivalent potentiometer also shown in the sole figure because it is obvious to substitute an art equivalent variable resistor as shown in the sole figure in place of a resistor also shown in the sole figure.

Regarding claims 5 & 12 Belfatto further teaches a resistor (sole fig. resistor 40) disposed between the pulse applying terminal (sole fig. source 34) and a ground (sole fig. resistor 40, wherein ground is on the left side of the resistor).

Regarding claims 15 & 16, Connerney further teaches the mixing means (fig. 1 mixers 60 & 62) further comprising an anti-parallel diode pair (fig. 2 diodes 62a, 62b & 60a, 60b, wherein fig. 2 is the same embodiment as fig. 1) including two diodes connected in parallel and opposite in direction to each other.

It would have been obvious to one having ordinary skill in the art at the time of the invention to have modified the mixer as taught in Belfatto with the diodes as taught in Connerney because it is obvious to substitute an art equivalent mixing

structure such as taught in Connerney in the place of the generic mixer shown in Belfatto.

Regarding claims 19 & 20, Connerney further teaches a second harmonic outputted from the first (fig. 2 diode 60b or 62b) of said two diodes (fig. 2 diodes 60a & 60b or 62a & 62b) being in opposite phase with a second harmonic outputted from the second (fig. 2 diode 60a or 62a) of said two diodes (wherein it is inherent that the second harmonic of each of the two diodes is going to be in opposite phase because the diodes are placed in anti-parallel configuration).

Regarding claims 25 & 26, Belfatto further teaches said voltage dividing means (sole fig. resistors 36,38,40) comprising a resistor (sole fig. resistor 38) disposed between the pulse applying terminal (sole fig. source 34) and the branching means (sole fig. branching means being the connection point between mixer 28 and resistor 38).

4. Claims 17, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Belfatto (US 4266201) and Connerney et al (US 4955079) as applied to claims 1 & 8 above, and further in view of Yamada et al (WO 03038992, cited by applicant).

Regarding claims 17 & 18, Belfatto and Connerney teach all of the elements as discussed above in claims 1 & 8, but fail to teach a band-pass filter that receives the output of said mixing means and permitting only the pulsed signal having a frequency even times a frequency of the local oscillation signal to pass therethrough and be outputted to the pulse output terminal.

Yamada teaches a band-pass filter (fig. on title page filter 23) that receives the output of said mixing means (fig. on title page mixer 25) and permitting only the pulsed signal (fig. on title page signal " $f_{IF} + 2 \times f_{LO}$ ") having a frequency even times a frequency of the local oscillation signal to pass therethrough and be outputted to the pulse output terminal (fig. on title page terminal 34).

It would have been obvious to one having ordinary skill in the art at the time of the invention to have modified the output terminal as taught in the above combination by adding the bandpass filter as taught by Yamada because the bandpass filter provides the benefit of passing frequencies within a desired frequency range and rejecting frequencies outside of the range.

5. Claims 21,22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Belfatto (US 4266201) in view of Connerney et al (US 4955079) as applied to claims 1 & 8 above, and further in view of Dobrovolny (US 20020022466).

Regarding claims 21 & 22, the combination of Belfatto and Connerney further teaches a voltage dividing means (Belfatto sole fig. resistors 38, 36, & 34) being

disposed between the mixing means (Belfatto sole fig. mixer 28) and a branching means (Belfatto sole fig. resistor 38 & mixer 28, wherein the connection path between the resistor 38 and the mixer 28 is a branching means), but fails to teach voltage dividing means comprising a parallel circuit comprising a resistor and a capacitor.

Dobrovolny teaches a voltage dividing means (fig. 1 biasing network resistor 26 & capacitor 28) comprising a parallel circuit comprising a resistor (fig. 1 resistor 26) and a capacitor (fig. 1 capacitor 28).

It would have been obvious to one having ordinary skill in the art at the time of the invention to have substituted the biasing resistors as taught in the above combination with the biasing network as taught in Dobrovolny because it is obvious to substitute an art equivalent biasing network such as taught in Dobrovolny in the place of the biasing network shown in the combination.

6. Claims 23 & 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Belfatto (US 4266201) in view of Connerney et al (US 4955079) as applied to claims 1 & 8 above, and further in view of Yamaji et al (US 5995819).

Regarding claims 23 & 24, the combination of Belfatto and Connerney teach all of the elements as discussed above in claims 1 & 8, but the combination fails to teach the circuitry further comprising a one-quarter wavelength short-ended stub connected to said mixing means such that said local oscillation signal is input into

said circuitry from said local oscillation wave input terminal via a connecting point between said mixer and said stub.

Yamaji teaches the circuitry (whole fig. 22) further comprising a one-quarter wavelength short-ended stub (fig. 22 stub 46) connected to said mixing means (fig. 22 series circuit 45) such that said local oscillation signal (fig. 22 signal "LO INPUT") is input into said circuitry from said local oscillation wave input terminal via a connecting point between said mixer and said stub.

It would have been obvious to one having ordinary skill in the art at the time of the invention to have modified the local oscillator input terminal as taught by the above combination by adding the short-ended stub as taught by Yamaji because the short-ended stub provides the benefit of appearing to be a short at direct currents and frequencies even times as large as the local oscillation frequency (col. 16 lines 17-19).

7. Claims 27 & 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Belfatto (US 4266201) in view of Connerney et al (US 4955079) as applied to claims 25 & 26 above, and further in view of Wheatley III et al (US 5530928).

Regarding claims 27 & 28, the combination further teaches said voltage dividing means (Belfatto sole figure Resistors 36,38,& 40) being disposed between the pulse applying terminal (Belfatto sole figure pulse source 34) and the branching

means (Belfatto sole figure mixer 28 & bias resistors 36,38,40, wherein the branching means is the connection path between resistor 38 and mixer 28), but fails to teach the voltage dividing means comprising a serial circuit that comprises a resistor and a diode.

Wheatley teaches the voltage dividing means (fig. 1 diode attenuator circuit resistors 16, 18, & 22 & diode 20) comprising a serial circuit that comprises a resistor (fig. 1 resistor 16) and a diode (fig. 1 diode 20).

It would have been obvious to one having ordinary skill in the art at the time of the invention to have substituted the bias resistors as taught by the above combination with the diode attenuator as taught by Wheatley because it is obvious to substitute an art equivalent signal level adjuster such as taught in the combination with another signal level adjuster as shown in Wheatley.

### ***Allowable Subject Matter***

8. Claims 7 & 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GERALD STEVENS whose telephone number is

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(571)270-5076. The examiner can normally be reached on Mon-Fri 7:30am - 5:00pm EST alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Pascal Bob can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

GDS

/Robert Pascal/  
Supervisory Patent Examiner, Art Unit 2817